substrate composition in the vertical dimension to achieve particular performance characteristics for the JFET.

FIG. **3**G shows an annealed dual gate MESFET structure having a deposited first gate **335** and an implanted second gate **330**. The MESFET requires only two implants, one for the buffer layer as previously described, and one for the second gate.

FIG. **4** shows a process flow diagram **400** for fabricating a dual gate structure for a JFET or MESFET. In step **405**, trenches are etched in the surface of a substrate. In step **410**, a sidewall spacer may be formed to establish the width of the region to be implanted for a first gate. In the absence of the sidewall spacer, the width of the implant region is essentially the width of the bottom of the trenches.

In step **415**, the first gate is formed. The gate may formed by depositing a metal to form a Schottky barrier on the bottom of the trench (e.g., for a MESFET), or an implant may be done to form a gate region with a p-n junction (e.g., for a JFET).

In step **420**, a second sidewall spacer may be formed to establish the width of a buffer region. The second sidewall spacer has a thickness that is greater than or equal to the thickness of the first sidewall spacer.

In step **425**, an implant is performed to form a buffer region beneath the first gate. The buffer region is implanted with a dopant that is of the same type as the substrate.

In step **430**, a sidewall spacer is formed for defining the width of a second gate. The sidewall spacer for the second gate is thicker than the sidewall spacer used for the first gate.

In step **435**, the second gate region is implanted using a high-energy low dose implant. The second implant produces a second gate that is narrower than the first gate and separated from the first gate by the buffer region.

In step **440**, the implants are annealed. The anneal may be done after all implants have been performed, or it may be done in stages. Piecewise annealing may be used when the second gate is implanted first, followed by the buffer implant. Once annealed, the deep implant will not be subjected to knock-on damage by subsequent shallower implants.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. For example, there are many combinations of the parameters for the implant and anneal process steps, and their sequencing, that may be used to produce the structures described herein. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

The invention claimed is:

1. A method for fabricating a dual gate structure for a field effect transistor (FET), said method comprising:

etching a gate trench in a surface of a semiconductor substrate;

forming a first gate region at the bottom of said gate trench, said first gate region continuous in a lateral direction parallel to said surface;

implanting a buffer region beneath said first gate region; and

implanting a second gate region beneath said buffer region, wherein said second gate region is formed entirely beneath said first gate region, and wherein, at a conclusion of implanting said second gate region, said second gate region is continuous in said lateral direction and is narrower than said first gate region.

2. The method of claim **1**, further comprising forming a sidewall spacer to establish a width of said first gate region.

3. The method of claim **1**, further comprising forming a sidewall spacer to establish a width of said buffer region.

4. The method of claim **1**, further comprising forming a sidewall spacer to establish a width of said second gate region.

5. The method of claim **1**, further comprising annealing said substrate subsequent to implanting said second gate region.

6. The method of claim **1**, further comprising annealing said substrate after said implanting said second gate region.

7. A method for fabricating a dual gate structure for a field effect transistor (FET), said method comprising:

in sequence,

etching a gate trench in a surface of a semiconductor substrate;

forming a first gate region at the bottom of said gate trench;

implanting a buffer region beneath said first gate region; and

implanting a second gate region beneath said buffer region, wherein said second gate region is formed entirely beneath said first gate region; wherein said first gate region and said second gate region together form said dual gate structure.

8. The method of claim **7**, further comprising forming a sidewall spacer to establish a width of said first gate region.

9. The method of claim **7**, further comprising forming a sidewall spacer to establish a width of said buffer region.

10. The method of claim **7**, further comprising forming a sidewall spacer to establish a width of said second gate region.

11. The method of claim **7**, wherein said first gate region is continuous in a lateral direction parallel to said surface, and said second gate region is continuous in said lateral direction and is narrower than said first gate region.

12. A method for fabricating a dual gate structure for a field effect transistor (FET), said method comprising:

etching a gate trench in a surface of a semiconductor substrate;

forming a first gate region at the bottom of said gate trench;

after forming the first gate region, implanting a buffer region beneath said first gate region; and

implanting a second gate region beneath said buffer region, wherein said second gate region is formed entirely beneath said first gate region; wherein said first gate region and said second gate region together form said dual gate structure.

13. The method of claim **12**, further comprising forming a sidewall spacer to establish a width of said first gate region.

14. The method of claim **12**, further comprising forming a sidewall spacer to establish a width of said buffer region.

15. The method of claim **12**, further comprising forming a sidewall spacer to establish a width of said second gate region.

16. A method for fabricating a dual gate structure for a field effect transistor (FET), said method comprising:

etching a gate trench in a surface of a semiconductor substrate;

forming a first gate region at the bottom of said gate trench;

implanting a buffer region beneath said first gate region; and